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Reference: Technical Progress Report (Combined reports No. 5 through 7)
Investigation of Lattice and Thermal Stress in GaN/AlGaN Field-Effect
Transistors
Period of Performance: 10/1/06 – 4/30/07
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In accordance with the requirements for Contract No. 0014-05-C-0120 entitled
"Investigation of Lattice and Thermal Stress in GaN/AlGaN Field-Effect Transistors,"
enclosed please find the combined technical progress report No. 5 through 7 for the
above period of performance.

Sincerely,

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Program Manager

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1.   Introduction

This report describes work performed in support of the program "Investigation of Lattice and Thermal Stress in GaN/AlGaN Field-Effect Transistors" (Contract No. N00014-05-C-0120) for the period 10/1/06 – 4/30/07.

Our overall goal is to understand the role and contribution of residual stress and junction temperature on the degradation of AlGaN/GaN HEMT electrical device characteristics. To execute this goal, electrical stress measurements will be performed on devices with varying residual stress, and under varying conditions. We plan to use the micro-Raman technique to monitor the evolution of residual stress in the active region of the device over time and under quiescent electrical bias. The question of whether a stress relaxation, potentially inducing dislocations, or simply changing the piezoelectric contribution to the 2DEG charge, contributes to device degradation will be investigated. We will seek to understand the influence of junction temperature on the magnitude of the stress at the active junction. The effect of physical, thermal, and electrical stress on device reliability will be investigated.

2.   Progress

2.1. Junction-Temperature Probing

A technique has been developed for thermal resistance measurement of thin film devices using the electrical properties of Schottky contacts on GaN HEMTs. This is a transient measurement technique, in which the Schottky gate thermionic characteristics are used to measure temperatures. Compared to Raman, this technique allows measurement of junction temperature directly under the gate. Since the junction temperature depends not only on the total power dissipated in the device, but also on the volumetric region within the device where the power is dissipated, this technique helps the understanding of the effect of electric field distribution in the channel on the junction temperature. For

example, the device may be biased in the linear regime, creating a uniform power dissipation condition in the channel, or in the saturation regime, creating a spatially non-uniform power dissipation condition. These two cases could be selected to dissipate the same total power, yet have been found by this measurement technique to produce significantly different junction temperatures.

Our technique first calibrates the gate-to-source forward I-V characteristics of the device under test as a function of temperature by mounting on a chuck at a known temperature and under vacuum to eliminate heat loss effects. The device is then pulsed to a pre-determined bias point for about 7 seconds and then turned off. A hundred milliseconds later, we force 1 μA of forward current into the gate and measure the gate voltage. The shift in voltage from the calibration curves is used to determine the junction temperature. Clearly the device has cooled slightly, and this technique does not provide the peak junction temperature. Nonetheless, this simple measurement enables us to measure a number of important thermal properties of the device and develop an accurate thermal model. In parallel, the temperature of a nearby device (sensor) can be continuously monitored, providing a direct measurement of the chip-scale thermal spreading properties of the material surrounding the device.

Both transient and steady state temperature measurements have been made. It is found that the electric field distribution under the gate has a profound effect on the measured temperature rise at fixed dissipated power or energy. Under high electric field conditions, the temperature at the gate is higher, presumably due to the electric field concentration resulting in a small power dissipation volume. At the condition of 0.55 Watts of instantaneous power dissipation, corresponding to dissipated energy of 3.865 Joules in the channel, ~44% higher temperature rise is measured under a high field condition. This observation is consistent with expected higher electric field concentration under the gate. Thermal spreading measurements indicate a thermal resistance of ~25°C/W per mm between the two sensors located at ~450 μm and ~225 μm from the heater device. Purely field-dependent memory effects, like charging, are confirmed to be negligible by measuring the gate characteristics after pulsing to a high-voltage low-current bias condition, resulting in minimal temperature rise due to little power dissipation. Fig. 2.1 shows the forward voltage characteristics of the Schottky gate diode used to provide a direct measurement of temperature in the gate region of the device. The diode stability and robustness was ensured via a 100 hour soak test at ~200°C, and via 20 power cycles. The temperature of the heater device was recorded after ~105 ms at the end of the power pulse, while sensor devices located at ~425 μm and ~225 μm were monitored continuously. Fig. 2.2 illustrates the typical temperature rise recorded at the sensor device for two different values of the drain-to-source voltage and at ~100 mA of drain current at the heater device. The pulse width of the heating pulse was varied from 1 to 5 seconds. The effect of electric field concentration under the gate, resulting in highly local power dissipation region, is clearly evident in temperature measurements shown in Fig. 2.3. Fig. 2.4 shows the thermal spreading characteristics of the device via temperature measurements on two sensors located at different distances.
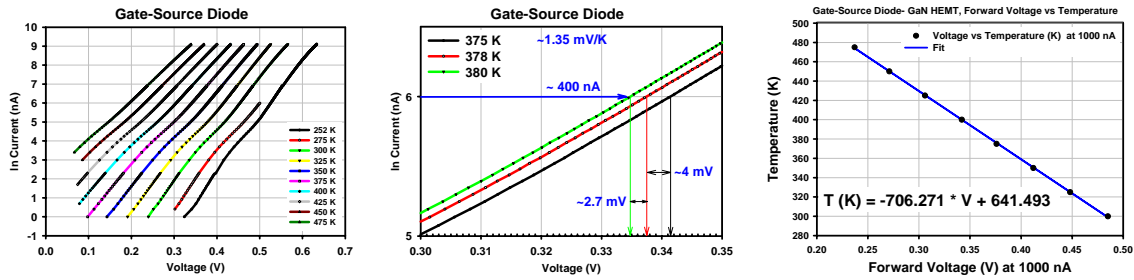
Fig.2.1. Gate-source Schottky diode calibration characteristics of a typical GaN HEMT device as a function of temperature (left) provides a temperature resolution of <1°C (middle). A gate-source probe current of 1 µA is used in subsequent measurements, which shows a linear dependence of forward diode voltage on temperature (right).
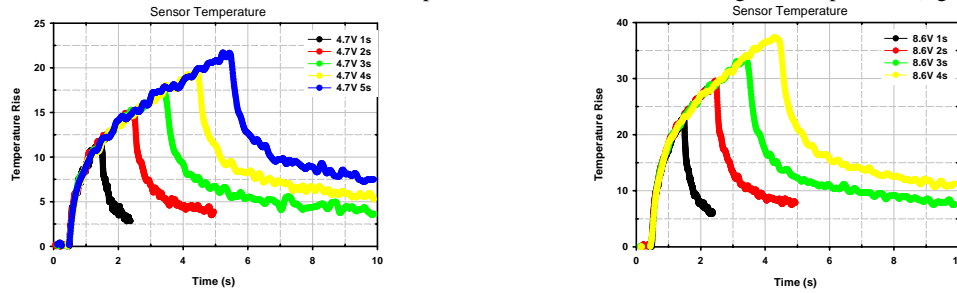
Fig. 2.2. Temperature-rise above ambient at the gate of the sensor HEMT device located ~425 microns from the heater GaN HEMT device. The drain-to-source pulse width at the heater device is varied from 1-5 seconds for two different values of the drain-to-source voltage (4.7V and 8.6V), while the heater drain current is held constant at ~100 mA.
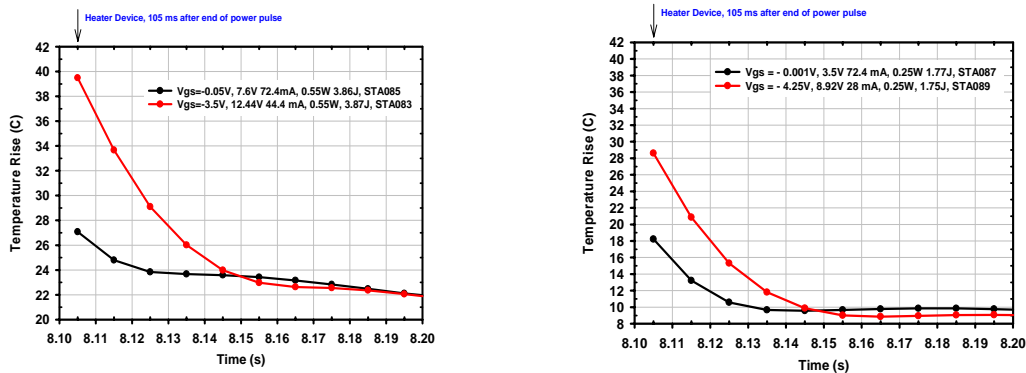
Fig.2.3. Temperature-rise above ambient at the gate of the heater device under two different electric field concentrations, as noted in the annotations. The two electric field conditions were chosen to enforce similar power (~0.55 Watts) and energy (~3.865 Joules) dissipation on exactly the same heater device (left). A similar effect was observed under a lower total power dissipation condition (right).
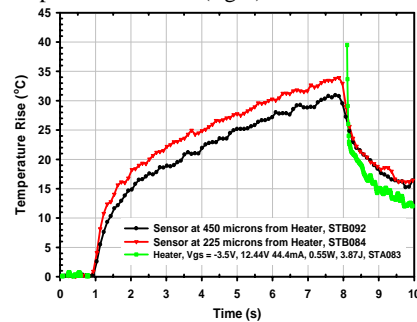

Fig. 2.4. Temperature-rise above ambient at the gate of the heater device and two sensor devices located at ~450 µm and ~225 µm away, indicating a thermal spreading resistance of ~25°C/W-mm between the sensor devices.

2.2. Controlled Stress Generation in GaN HEMT Dies

Controlled stress generation in GaN-on-SiC will be used to study the effect of variable physical stress on electrical performance and degradation of GaN HEMTs. To this end, we have constructed a setup, which will be used to apply variable physical stress on GaN die and allow electrical measurements of devices in the die under stress.

Given the low load requirements combined with high load accuracy, a system with a voice coil actuator was designed and built to controllably induce the desired amount of stress. The produced force depends directly on the electrical current in the coil. The test die is mounted in a specially designed package with a cutout on the bottom. A dedicated printed circuit board with a section removed under the package and mechanical attachments for the load frame as well as electrical attachments is used to mount the modified package. The 3D drawings of the test frame and the package are shown in fig. 2.5 and the actual test frame and board with modified package are shown in figure 2.6. We will use this test frame to perform the controlled stress experiment on GaN HEMT devices.
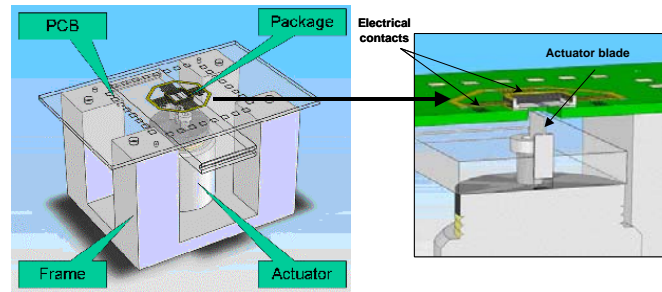
Figure 2.5 3D drawings of the test frame and the package constructed for use in the controlled stress experiment.
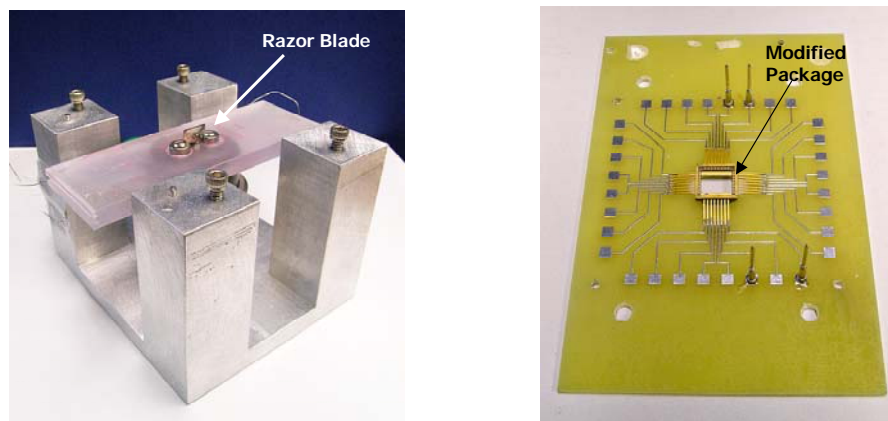
Figure 2.6 (Left) Picture of the constructed setup showing the actuator retrofitted with a razor blade to apply the stress on the GaN die. (Right) Circuit board constructed to fit in the stress setup is shown with the modified package for mounting GaN HEMT die.

3.   Financial Status

Figure 3.1 is a plot of the program's financial status as of 30 April 2007. The program is fully funded at $249,963, and includes a 6-month no cost extension. The actuals are approximately $147K as of 30 April 2007. We expect spending to continue at a rate of ~$25K/mo for the remainder of the program.

Figure 3.1 Quarterly funds report.

4.   Plans for the next quarter

We plan to perform additional measurements using the pulsed temperature probing technique to confirm the measured results. We plan to complement the measurement results using Micro-Raman temperature measurements as well. We also plan to characterize GaN devices under physical stress and quantify the impact of this stress on the electrical performance, as well as the electrical degradation of GaN devices.